WHAT IS CLAIMED IS:

1. An interface logic circuit for coupling a domain output of a first logic circuit domain to a domain input of a second logic circuit domain comprising:

a first cut-circuit powered by first and second voltage potentials and having a first input coupled to the domain output, and a first output coupled to the domain input, wherein the first voltage potential is coupled to the first cut-circuit in response to a first logic state of a first control signal and decoupled from the first cut-circuit in response to a second logic state of the first control signal; and

a latch circuit having a latch input coupled to the first input, and a latch output coupled to the first output, wherein the latch circuit latches logic states at the domain input when the first voltage potential is decoupled from the first cut-inverter.

2. The interface logic circuit of claim 1, wherein the latch circuit is powered by the second voltage potential and a third voltage potential, and the third potential is coupled to the latch circuit in response to the second logic state of the first control signal and decoupled from the latch circuit in response to the first logic state of the first control signal.

3. The interface logic circuit of claim 2, wherein the second voltage potential is coupled to the first cut-circuit in response to the second logic state of a second control signal and decoupled from the first cut-circuit in response to the first logic state of the second control signal.

4. The interface logic circuit of claim 3, wherein the second voltage potential is coupled to the latch circuit in response to the first logic state of the second control signal and decoupled from the latch circuit in response to the second logic state of the second control signal.

5. The interface circuit of claim 1, wherein the first cut-circuit comprises:

an inverter stage having an inverter input coupled as the input of the first cut_inverter, an inverter output coupled as the output of the first cut_inverter, a first power supply node, and a second power supply node coupled to the second voltage potential; and

a first electronic switch coupling the first voltage potential to the first power supply node in response to the first logic state of the first control signal and decoupling the first voltage potential from the first power supply node in response to the second logic state of the first control signal.

6. The interface circuit of claim 5, wherein the latch circuit comprises:

a first inverter having a first inverter input as the latch input and a first inverter output as the latch output; and

a second cut-inverter having an input coupled to the latch output, an output coupled to the latch input, wherein the third voltage potential is coupled to the first cut-inverter in response to the second logic state of a first control signal and decoupled from the second cut-inverter in response to the first logic state of the first control signal.

7. The interface circuit of claim 6 further comprising a second electronic switch coupling the second voltage potential to the second power supply node in response to the second logic state of a second control signal and decoupling the second voltage potential from the second power supply node in response to the first logic state of the second control signal.

8. The interface circuit of claim 5, wherein the inverter stage comprises

an N channel field effect transistor (NFET) having a gate coupled to the inverter input, a source coupled to the second power supply node, and a drain coupled to inverter output; and

a P channel field effect transistor (PFET) having a gate coupled to the inverter input, a source coupled to the first power supply node, and a drain coupled to the inverter output.

9. The interface circuit of claim 5, wherein the first electronic switch is a PFET having a gate coupled to the first control signal, a drain coupled to the first power supply node, and a source coupled to the first voltage potential.

10. The interface circuit of claim 7, wherein the second electronic switch is an NFET having a gate coupled to the second control signal, a drain coupled to the second power supply node, and a source coupled to the second voltage potential.

11. The interface circuit of claim 6, wherein the second cut-inverter comprises:

an inverter stage having an inverter input coupled as the input of the second cut_inverter, an inverter output coupled as the output of the second cut_inverter, a first latch power supply node, and a second latch power supply node coupled to the second voltage potential; and

a third electronic switch coupling the third voltage potential to the first latch power supply node in response to the second logic state of the first control signal and decoupling the third voltage potential from the first latch power supply node in response to first logic state of the first control signal.

12. The interface circuit of claim 11 further comprising a fourth electronic switch coupling the second voltage potential to the second latch power supply node in

response to the first logic state of the second control signal and decoupling the second voltage potential from the second latch power supply node in response to the second logic state of the second control signal.

13. The interface circuit of claim 11, wherein the inverter stage comprises:

an N channel field effect transistor (NFET) having a gate coupled to the inverter input, a source coupled to the second power supply node, and a drain coupled to inverter output; and

a P channel field effect transistor (PFET) having a gate coupled to the inverter input, a source coupled to the first latch power supply node, and a drain coupled to the inverter output.

14. The interface circuit of claim 11, wherein the third electronic switch is an PFET having a gate coupled to a logic inversion of the second control signal, a drain coupled to the first latch power supply node, and a source coupled to the third voltage potential .

15. The interface circuit of claim 12, wherein the fourth electronic switch is an NFET having a gate coupled to a logic inversion of the first control signal, a drain coupled to the second latch power supply node, and a source coupled to the second voltage potential.

16. The interface logic circuit of claim 11, wherein the first logic circuit domain is a cut-domain with power-gated circuitry and the second domain is a non-cut-domain without power-gated circuitry.

17. The interface logic circuit of claim 16, wherein a voltage potential is coupled to the power-gated circuitry in the cut-domain in response to the first logic state of the

first control signal and decoupled from the power-gated circuitry in response to the second logic state of the first control signal.

18. The interface circuit of claim 1, wherein the latch circuit comprises:

a first inverter circuit having a first inverter input as the latch input and a first inverter output as the latch output; and

a second inverter circuit having an second inverter input coupled to the first inverter output and a second inverter output coupled to the second inverter output.

19. The interface circuit of claim 2, wherein the first and third voltage potentials are equal.

20. A data processing system comprising:

a central processing unit (CPU);

a random access memory (RAM);

an input output (I/O) interface unit; and

a bus for coupling the CPU, RAM and I/O interface unit, the CPU having first and second logic circuit domains and an interface logic circuit for coupling a domain output from the first logic circuit domain to a domain input to the second logic circuit domain, the interface circuit including a first cut-circuit powered by first and second voltage potentials and having a first input coupled to the domain output, and a first output coupled to the domain input, wherein the first voltage potential is coupled to the first cut-circuit in response to a first logic state of a first control signal and decoupled from the first cut-circuit in response to a second logic state of the first control signal, and a latch circuit having a latch input coupled to the first input, and a latch output coupled to the first output, wherein the latch circuit latches logic states at the domain input when the first voltage potential is decoupled from the first cut-inverter.

21. The data processing system of claim 20, wherein the latch circuit is powered by the second voltage potential and a third voltage potential, and the third potential is coupled to the latch circuit in response to the second logic state of the first control signal and decoupled from the latch circuit in response to the first logic state of the first control signal.

22. The data processing system of claim 21, wherein the second voltage potential is coupled to the first cut-circuit in response to the second logic state of a second control signal and decoupled from the first cut-circuit in response to the first logic state of the second control signal.

23. The data processing system of claim 22, wherein the second voltage potential is coupled to the latch circuit in response to the first logic state of the second control signal and decoupled from the latch circuit in response to the second logic state of the second control signal.

24. The data processing system of claim 21, wherein the first and third voltage potentials are equal.